Electronic Version
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Description

METHOD FOR DETERMINING INTEGRITY OF MEMORY

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a method for determining the integrity of memory and more particularly, to a method for determining the integrity of defective memory under a plurality of operating environments.

[0003] 2. Description of the Prior Art

[0004] An essential component in today's electronic devices, such as switches, routers, or the like, is memory, such as a header table or a packet buffer. Because of the important role that memory plays in electronic devices, it is standard practice to only use memory that is free from defects in electronic devices. However, it is not to say that memory must be defective free in order to be incorporated for use. Given the right techniques, manufacturers could use

memory with defective sections in a product and still have the product retain the same functionality as a product that uses defective free memory.

[0005] However, before a defective memory is employed in the use of a product, a manufacturer should be certain about the memory's integrity. That is to say, a manufactured memory should have consistency throughout a certain range of operating environment condition settings. In this case, a memory with integrity is a memory in which the number of defects and their respective locations are consistent under all the operating environments an electronic device is intended to perform under. For example, imagine a product is intended to run under two operating environments in regards to a voltage condition - low and medium. After testing processes it is discovered that a defective memory that the manufacturer plans to use in the product has two defects one at section 1, the other at section 5 - when under a low voltage environment. In order for the memory to be declared as having integrity, the memory would have the two defects at the same sections when under a medium voltage environment. Any other case, and the memory lacks integrity (For example, there are three defects under the medium voltage, or there are

two defects but one is at section 3 and the other at section 6).

[0006] A defective memory's integrity is important to check because a defective memory lacking integrity and used in an electronic device can cause operating problems in the electronic device. For example, imagine a memory lacking integrity is used inside a switch, such as a header table memory or a packet buffer memory used in a switch; the number of defects increases when the circuits (including the memory) of the switch operate above a threshold temperature. When the switch is first turned on, the circuits are below the threshold temperature. However, after operating for a certain amount of time, the circuits of the switch reach the threshold temperature. The switch then tries to access a section of the memory that was accessible when under the threshold temperature but now has become defective because the threshold temperature has been reached, resulting in malfunction, e.g. difficulty in forming and utilizing a linked list associated with the header table or the packet buffer.

SUMMARY OF INVENTION

[0007] It is therefore one of the many objectives of the claimed invention to provide a method for testing the integrity of a

memory with defective sections under a plurality of operating environments.

[0008] According to the claimed invention, a method for testing the integrity of a memory with defective sections under a plurality of operating environments is disclosed. The claimed method for determining the integrity of a memory under a plurality of operating environments comprises: setting a current operating environment out of the plurality of operating environments for a condition to be tested; testing the memory under the current operating environment; recording a result of the testing step for the current operating environment; and comparing the recorded result for the current operating environment with a recorded result for a previous operating environment.

[0009] The claimed invention provides a method of testing the integrity of memory with defective sections. As one of the many advantages in using the claimed invention, manufacturers can confidently employ the use of memory with defective sections in their products and still have the product perform reliably. As a result, manufacturers can improve the amount of memory deemed usable after each fabrication, thus leading to lowered costs and increased efficiency.

[0010] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0011] Fig.1 is a block diagram of a memory to be tested according to an embodiment of the present invention.

[0012] Fig.2 is a diagram of a flowchart of a method employed according to an embodiment of the present invention.

[0013] Fig.3 is a block diagram of a status record memory and the memory of Fig.1 according to an embodiment of the present invention.

Detailed Description

[0014] Please refer to Fig.1. Fig.1 is a block diagram of a memory to be tested according to an embodiment of the present invention. The memory 10 in Fig.1 is to be taken as an example for the memory referred to in Fig.2 and Fig.3. For actual applications, the memory 10 can be a header table, a packet buffer in a switch, or the like. The memory 10 is divided into N sections. As stated earlier, the present invention provides a method for testing the integrity of a

memory with defective sections under a plurality of operating environments for a given condition. The condition and number of operating environments to be tested are left for the tester to decide. For example, the tester may choose to test two conditions - voltage and temperature. Under each condition, the tester may choose 3 operating environments - low, medium, and high. The tester can choose to be even more specific when listing operating environments by listing values such as 1.8 volts, 3.3 volts, and 5 volts for voltage or 65 degrees, 100 degrees, and 130 degrees for temperature. These should only be taken as examples and not a limitation of the present invention.

[0015] Please refer to Fig.2. Fig.2 is a diagram of a flowchart of a method employed according to an embodiment of the present invention. It is assumed prior to the steps listed that the tester has already chosen the condition and the corresponding number of operating environments. In this embodiment of the present invention the steps are as follows. For details concerning the built-in self test (BIST), please refer to "a programmable BIST core for embedded DRAM",by Huang et. al.,IEEE Design and Test Magazine, Jan-Mar 1999, which is incorporated herein by reference.

[0016] Step 200:Start.

[0017] Step 210:Set Operating Environment. The testing system sets up the current operating environment that the memory 10 is to be tested under as one of a plurality of operating environments. Each time this step is executed, a different operating environment is set up.

[0018] Step 220:Test Memory. The memory 10 is tested to detect the number of defects present in the memory 10 and their respective locations. This testing step can be embodied, as one example, by applying a built-in self test (BIST) on the memory 10.

[0019] Step 230:Record Results. The results of the test are recorded so that they can be compared with results from other tests in other operating environments. These test results recorded in this step are known as current test results.

[0020] Step 240:Additional Operating Environments? The testing system checks if there are other additional operating environments to be checked. If there are, then that means the test is not over, and the testing system returns to Step 210. Otherwise it means that the test is over, and go to step 250.

[0021] Step 250:Compare results. The testing system compares the results of all tests. If results match, go to step 260.

Otherwise, go to step 270.

[0022] Step 260:Pass. The memory 10 has passed all the operating environment tests and therefore, declared as having integrity. The memory 10 is suitable for use in an electronic device.

[0023] Step 270:Fail. The number and/or location of defective sections in the memory 10 is not consistent and therefore, declared as not having integrity. The memory 10 is not suitable for use in an electronic device.

[0024] Step 280:Finish.

[0025] To illustrate, assume that a memory 10 divided into N sections is being tested under the condition of voltage with the operating environments of low, medium, and high to be tested in that order. The testing system begins by setting the operating environment for low voltage (step 210). Then, the memory 10 is tested (step 220) and the results recorded (step 230) assume that the testing system finds one defect present at section 1. Next, the testing system checks if there are any additional operating environments to be tested left untested (step 240). Since this is the first time through and there still exist two additional operating environments of medium voltage and high voltage, the testing system returns to set the operat-

ing environment.

[0026] This time the testing system will set the operating environment for medium voltage (step 210). The memory 10 is tested (step 220) and the results recorded (step 230). Now assume that the medium voltage test yields one defect at section 1. Again in step 240 since still one additional operating environment is found left untested, steps 210, 220, and 230 are performed once again for the operating environment of high voltage, and a corresponding result is stored.

[0027] After having these tested result stored, the testing system will find there is not more operating environments left to be tested (step 240). As a result the testing system proceeds to compare if the testing results stored for various operating environments, which in this embodiment are low voltage, medium voltage, high voltage, match with one another (step 250). If the above testing result for high voltage also reads one defect at section 1 and the results for these operating environments match, the memory 10 is then deemed to have passed the process and as having integrity (step 260). The memory 10 therefore can be used in an electronic device. However for example, if the above testing result for high voltage yields an additional defect

at section 8 and the results for these operating environments do not match, the memory 10 is deemed as not having integrity and therefore, not usable in an electronic device (step 270).

[0028] Please note, that the method diagramed in Fig.2 should not be taken as limitations; the illustrated serves merely as an example. Also note that the condition of voltage and temperature along with the operating environments of low, middle, and high are also merely examples, which means testing methods incorporating other conditions concerning operating environment testing, or a combination thereof, that one skilled in the art will appreciate, also fall into scope of the claimed invention.

[0029] For step 220 described above, according to an embodiment of the present invention, the BIST can be performed on the memory 10 associated with a status record memory 20, as shown in Fig.3. As shown in Fig.3 each section of the status record memory 20 corresponds to one section of the memory 10 and serves to record the defective status of that corresponding section of the memory 10. In this embodiment after the BIST is performed, the sections of the status record memory 20 corresponding to detected defective sections of the memory 10 will be

marked, as shown in Fig.3 a crossed out section to indicate a defective status. Then the recording step 230 can be implemented by recording the content of the status record memory 20.

[0030] In this embodiment, the testing data of the BIST are inputted by the testing system to the electronic device (for example, an integrated circuit chip) having the memory to be tested via a plurality of I/O interfaces (for example, pins of the IC chip) of the electronic device. The comparing step of step 250 may be performed, without limitation, by an embedded comparing circuitry fabricated in the electronic device. The comparing result may be latched in a built-in register of the electronic device for later pass/fail indication use.

[0031] The present invention provides a method of testing the integrity of memory with defective sections. By employing this method, manufacturers can confidently employ the use of memory with defective sections in their products and still have the product perform reliably. As a result, manufacturers can improve the amount of memory deemed usable after each fabrication, thus leading to lowered costs and increased efficiency.

[0032] Those skilled in the art will readily observe that numerous

modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, that above disclosure should be construed as limited only by the metes and bounds of the appended claims.